

## **AMENDMENTS TO THE CLAIMS:**

### **Complete Listing of Claims**

1           1. (original) A bit-rate detection circuit, comprising:  
2           a plurality of shift registers adapted to serially shift in bits of data having a  
3 data frequency from a first transceiver, said shift registers being clocked at a first  
4 predetermined rate; and  
5           logic circuitry responsively coupled to said shift registers providing an  
6 output signal indicative of the data frequency.

1           2. (original) The bit-rate detection circuit of Claim 1 wherein said first  
2 predetermined rate is the highest possible data rate that the incoming data  
3 frequency can be.

1           3. (original) The bit-rate detection circuit of Claim 1 wherein said logic  
2 circuitry is coupled to nodes defined between said shift registers.

1           4. (original) The bit-rate detection circuit of Claim 3 wherein said logic  
2 circuitry comprises a first logic set and a second logic set each providing an  
3 output signal, said first logic set being coupled to a first set of said nodes  
4 between said shift registers, and said second logic set being coupled to a second  
5 set of said nodes between said shift registers.

1           5. (original) The bit-rate detection circuit of Claim 4 wherein said first  
2 logic set determines if said incoming data frequency is a first predetermined  
3 frequency, and said second logic set determines if said incoming data frequency  
4 is a second predetermined frequency being less than said first predetermined  
5 frequency.

1           6. (original) The bit-rate detection circuit of Claim 5 wherein said first  
2 predetermined frequency is a multiple of said second predetermined frequency.

1           7. (original) The bit-rate detection circuit of Claim 4 further comprising  
2 output logic circuitry responsively coupled to said first logic set and said second  
3 logic set, said output logic circuitry providing said output signal indicative of the  
4 data frequency.

1           8. (original) The bit-rate detection circuit of Claim 4 further comprising a  
2 third logic set coupled to a third set of said nodes being different than said first  
3 and second sets of nodes.

1           9. (original) The bit-rate detection circuit of Claim 8 wherein said third  
2 logic set determines if said incoming data frequency is a third predetermined  
3 frequency being less than said second predetermined frequency.

1           10. (original) The bit-rate detection circuit of Claim 9 wherein said first  
2 predetermined frequency is in multiple of said third predetermined frequency.

1           11. (original) The bit-rate detection circuit of Claim 10 wherein said third  
2 predetermined frequency is also a multiple of said second predetermined  
3 frequency.

1           12. (original) The bit-rate detection circuit of Claim 1 further comprising a  
2 communications transceiver module responsively coupled to said logic circuitry  
3 output signal and adapted to transmit data back to said first transceiver at said  
4 incoming data frequency.

1           13. (original) The bit-rate detection circuit of Claim 1 wherein said logic  
2 circuitry includes a single clock operating at a first frequency.

1           14. (original) The bit-rate detection circuit of Claim 1 wherein said logic  
2 circuit provides said output signal as a function of framing data clocked into said  
3 shift registers.

1           15. (original) The bit-rate detection circuit of Claim 14 wherein said  
2 framing data is A1 and A2 SONET framing bytes.

1           16. (original) A data transceiver, comprising:  
2 a data receiver circuit;  
3 logic circuitry responsively coupled to said receiver circuit determining a  
4 data rate of data received by said data receiver, said logic circuit including and  
5 operating off a single clock operating at a first predetermined frequency; and  
6 a data transmitter responsively coupled to said logic circuitry and adapted  
7 to transmit data at a data rate as a function of said output signal.

1           17. (original) The bit-rate detection circuit of Claim 16 wherein said logic  
2 circuitry comprises;

3           a plurality of shift registers adapted to serially shift in data having a data  
4 frequency from a first transceiver, said shift registers being clocked at a first  
5 predetermined rate; and

6           logic circuitry responsively coupled to said shift registers providing an  
7 output signal indicative of the incoming data frequency.

1           18. (original) The bit-rate detection circuit of Claim 17 wherein said first  
2 predetermined rate is the highest possible data rate that the incoming data  
3 frequency can be.

1           19. (original) The bit-rate detection circuit of Claim 17 wherein said logic  
2 circuitry is coupled to nodes defined between said shift registers.

1           20. (original) The bit-rate detection circuit of Claim 19 wherein said logic  
2 circuitry comprises a first logic set and a second logic set each providing an  
3 output signal, said first logic set being coupled to a first set of said nodes defined  
4 between said shift registers, and said second logic set being coupled to a second  
5 set of said nodes defined between said shift registers.

1           21. (original) A method of detecting a bit-rate of data incoming to a  
2 receiver, comprising the steps of:

3           a) clocking said incoming bit data at a first frequency into a  
4 plurality of shift registers having a node between each said shift register; and

5           b) analyzing data at a plurality of said nodes to determine the bit-  
6 rate of said incoming bit data.

1           22. (original) The method as specified in Claim 21 wherein said first  
2 frequency is the maximum possible data bit-rate of said incoming bit data.

1           23. (currently amended) The method as specified in Claim 22 wherein  
2 logic circuitry analyzes said bit data, said logic circuitry having a first logic set  
3 coupled to a first set of said nodes determining if said data bit-rate could be a  
4 first data rate, and a second logic set coupled to a second set of said nodes  
5 determining if said data bit-rate could be a second data rate being less than said  
6 first data rate.

1           24. (original) The method of Claim 23 wherein said first data rate is said  
2 first frequency, and said first data rate is also a multiple of said second data rate.

1           25. (original) The method of Claim 21 further comprising the step of  
2 responsively transmitting data from a transmitter at a data rate being said  
3 determined incoming data bit-rate.

1           26. (original) The method of Claim 21 wherein frame data is said  
2 analyzed data in said step b).

1           27. (original) The method of Claim 26 where in said frame data is a A1  
2 and A2 SONET framing byte.

1           28. (original) A bit-rate detection circuit, comprising:  
2           a plurality of shift registers adapted to shift in bits of data having a data  
3 rate in parallel from a first transceiver, said shift registers being clocked at a  
4 predetermined clock rate; and  
5           logic circuitry responsively coupled to said shift registers providing an  
6 output signal indicative of the data rate.

1           29. (original) The bit-rate detection circuit as specified in Claim 28,  
2 wherein said clock rate is less than the maximum data rate.

1           30. (original) The bit-rate detection circuit as specified in Claim 29,  
2 wherein said data rate is a multiple of said clock rate.